Couunter design:

`timescale 1ns / 1ps

// Description: 4 bit counter with source clock (100MHz) division.

module counter\_clk\_div(clk,rst,counter\_out);

input clk,rst;

reg div\_clk;

reg [25:0] delay\_count;

output reg [3:0] counter\_out;

//////////clock division block////////////////////

always @(posedge clk) begin

if(rst) begin

delay\_count<=26'd0;

div\_clk <= 1'b0; //initialise div\_clk

end

else

if(delay\_count==26'd212) begin

delay\_count<=26'd0; //reset upon reaching the max value

div\_clk <= ~div\_clk; //generating a slow clock

end

else begin

delay\_count<=delay\_count+1;

end

end

/////////////4 bit counter block///////////////////

always @(posedge div\_clk) begin

if(rst) begin

counter\_out<=4'b0000;

end

else begin

counter\_out<= counter\_out+1;

end

end

endmodule





